Midterm Review

Logistics
- "60 minute" exam you have 90m
- Forward Progress only
- 8am - 8pm Pacific
  6:30

How to review
1. HW
2. In-class quiz Q's
3. Working sample problems
4.) Re-watching lecture?
5.) Re-watch 5 chunks

ADD and SUB

How many instructions does the machine support?

$2^6 = 64$ operations

63: I and S type instructions
1: R type
2: 64 functions

$63 + 64 = 127$ instructions

HW 1 Q6a.

R-type

1. Expand instruction to 32 bits wide
   - 64 instructions
   - 64 registers $\Rightarrow$ 2^6
   - 6610
   - $2^5 = 32$ registers

2. Reduce 'char' to 24 bits
   - to expand rs, rt, rd to 6 bits each.
Forwarding

1. add $1, $2, 100
2. sub $3, $4, $5
3. lw $4, 100($3)
4. sw $3, 100($5)
5. add $6, $7, $8

<table>
<thead>
<tr>
<th></th>
<th>Single Cycle</th>
<th>Multi Cycle</th>
<th>Pipelined</th>
</tr>
</thead>
<tbody>
<tr>
<td>CT</td>
<td>latency of the worst-case instruction</td>
<td>latency of the worst-case sub-part of machine</td>
<td>worst-case pipeline stage</td>
</tr>
<tr>
<td>through put</td>
<td>1 inst/lcycle</td>
<td>1 inst/5 cycles</td>
<td>1 inst/lcycle</td>
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</table>

HW 1, Q 8

\[ 35 + 25 = 60\% \text{, avg. } 0.6 \text{ writers/cycle} \]

HW 4, Q 6

35% with 1590 br, 25% lw, 25% sw/cr

Reg file writes/cycle? Pipeline never stalls.

WB stage only thing that writes to the reg file.

Q: really: which inst types write the reg file?

HW 1, Q 8

\[ e = A[4] \rightarrow x2; \]

Assume A is char

Assume A is int

Assume A is uint16 or char

Assume A is uint32 or int

Branch Range

\[ 0 \text{ to } 2^{16} \]