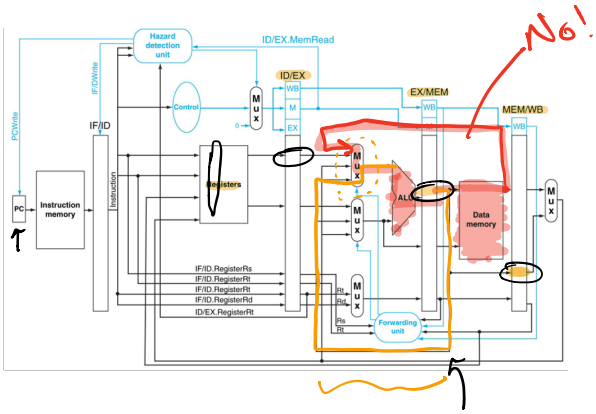


Midterm Review

Logistics

- "80 minute" exam you have 90m
- Forward Progress only
- 8am - 8pm US / Pacific
  - 6:30

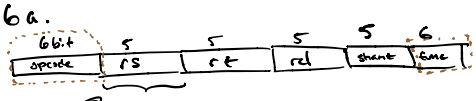
How to review

1.) HW
2.) In-class quiz Q's
3.) Working book problems
4.) Re-watching lecture's whole chunks
6.(5.) Re-watching lecture's

ADD and SUB

How many instructions does the machine support? HW 1 Q6a.

R-type



5 bits

66 bits

$2^5 = 32$ registers

64 registers => 2^6

$2^6 = 64$ operations 76 bits

63 I and J type instructions

1 R type

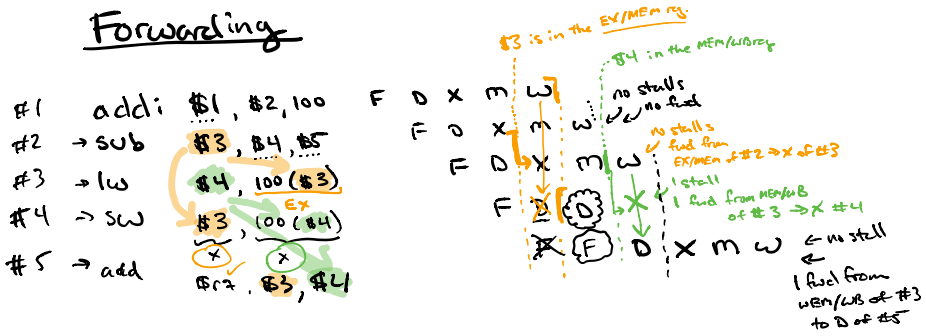
$\rightarrow 2^6$ functions

$\rightarrow 63 + 64 = 127$ instructions

1.) Expand instruction to 35 bits wide

* 2.) Reduce 'shamt' to 26 bits to expand rs, rt, rd to 6 bits ea.

Forwarding



	Single Cycle	Multi Cycle	Pipelined
CT	latency of the worst-case instruction	latency of the worst-case sub-part of machine → worst-case pipeline stage	
throughput	1 inst / 1 cycle	1 inst / 5 cycles	1 inst / 1 cycle

HW4 Q6

35% arith, 15% br, 25% lw, 25% store

Reg file writes/cycle? Pipeline never stalls.

WB stage only thing that writes to the reg file.

Q is really: which inst types write the reg file?

35 + 25 = 60%, avg. 0.6 writes / cycle

HW 1 Q8

```
c = A[4] >> 2;
```

$t1 = A
$s1 = c

type of A?

A is uint8_t or char
A is uint32_t or int

Assume A is type char

```
lw  $t2, 4($t1)
slr $t2, $t2, 2
sw  $t2, 0($s0)
```

Assume A is type int

```
lw $t2, 16($t1)
```

Branch Range