CSE 141: Introduction to Computer Architecture

Instruction Set Architecture (ISA)
What is Computer Architecture?

Computer Architecture =

Instruction Set Architecture +

Machine Organization

*How you talk to the machine*

*What the machine hardware looks like*
An Instruction Set Architecture is an abstraction of a computational machine

- An ISA is “the agreed-upon interface between all the software that runs on the machine and the hardware that executes it.”
Computers do not speak English
And they do not speak C or Java or Python or Haskell (or...) either

```
Specification
Programmer
High Level Language
(C, Java, Rust, etc)
Compiler
Assembly Language
Assembler
Machine Language
Machine Interpretation
Control Signal Spec
```

```
“Swap two array elements.”

int temp = array[index];
array[index] = array[index + 1];
array[index + 1] = temp;

lw $15, 0($2)  
lw $16, 4($2)  
sw $16, 0($2)  
sw $15, 4($2)

10001100011000100000000000000000  
1000110011110010000000000000100  
10101100111100100000000000000000  
1010110001100010000000000000100

ALUOP[0:3] <= InstReg[9:11] & MASK
```
Poll Q: If you had to put the ISA somewhere in this stack, would you say it sits between...

- Specification and HLL
- HLL and assembly
- Assembly and machine language
- Machine language and control signals
- ISAs define control signals

```
int temp = array[index];
array[index] = array[index + 1];
array[index + 1] = temp;
```

```
lw $15, 0($2)
lw $16, 4($2)
sw $16, 0($2)
sw $15, 4($2)
```

```
0001 0001 0001 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000
0001 0001 0001 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000
0101 0001 0001 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000
0101 0001 0001 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000
```

```
ALUOP[0:3] <= InstReg[9:11] & MASK
```

“Swap two array elements.”
The Instruction Set Architecture

• that part of the architecture that is visible to the programmer
  – available instructions ("opcodes")
  – number and types of registers
  – instruction formats
  – storage access, addressing modes
  – exceptional conditions
The Instruction Execution Cycle

- **Instruction Fetch**
  - Obtain instruction from program storage

- **Instruction Decode**
  - Determine required actions and instruction size

- **Operand Fetch**
  - Locate and obtain operand data

- **Execute**
  - Compute result value or status

- **Result Store**
  - Deposit results in storage for later use

- **Next Instruction**
  - Determine successor instruction
A brief preview of some machine organization concepts:

**Cycle**

- The smallest unit of time in a processor
A brief preview of some machine organization concepts: **Parallelism**

- The ability to do more than one thing at once

Real-world example

ARM’s Thumb instruction set is (mostly) 16-bit instructions on a 32-bit machine

ISA design makes fetch “freely parallel”
A brief preview of some machine organization concepts: 

**Superscalar Processor**

- Can execute more than one instruction per cycle

```
Instruction
  Fetch

Instruction
  Decode

Operand
  Fetch

Execute
  Fetch

Duplicate is easy but expensive...

How to do parallelism well?
- Second half of this class
- CSE148
```
A brief preview of some machine organization concepts: *Pipelining*

- Overlapping parts of a large task to increase throughput without decreasing latency
  - Key insight: The less work you do in one step, the faster each step can finish
Key questions to ask when designing an ISA

- operations
  - how many?
  - which ones?
- operands
  - how many?
  - location
  - types
  - how to specify?
- instruction format
  - size
  - how many formats?

```
y = x + b
```

Syntax choice
```
add r5, r1, r2
add [r1, r2], r5
```

Design choice
```
add r5, r1–r4
```

how does the computer know what
0001 0101 0001 0010 means?
Let us design MIPS together

• We will look at several of the key ISA design decisions
• To succeed in 141 you need to understand the how and the why of MIPS
  – The rest of the course builds on MIPS, so need to be comfortable with it
  – But also need to understand the architectural tradeoffs of MIPS
• To succeed in 141L you need to understand the tradeoffs in ISA design
How long should an instruction be?

- Fixed
- Variable
- Hybrid

```
add r5, r1, r2
```
Instruction length tradeoffs

- **Fixed-length instructions (MIPS)**
  - easy fetch and decode
  - simplify pipelining and parallelism.

- **Variable-length instructions (Intel 80x86, VAX)**
  - multi-step fetch and decode
  - much more flexible and compact instruction set.

- **Hybrid instructions (ARM)**
  - Middle ground

⇒ All MIPS instructions are 32 bits long.
  - this decision impacts every other ISA decision we make because it makes instruction bits scarce.
Instruction Formats: What does each bit mean?

- Having many different instruction formats...
  - complicates decoding
  - uses more instruction bits (to specify the format)
  - Could allow us to take full advantage of a variable-length ISA

**VAX 11 instruction format**

<table>
<thead>
<tr>
<th>Byte 0</th>
<th>1</th>
<th>n</th>
<th>m</th>
</tr>
</thead>
<tbody>
<tr>
<td>OpCode</td>
<td>A/M</td>
<td>A/M</td>
<td>A/M</td>
</tr>
</tbody>
</table>

- **register disp**
  - 5 r
  - A r byte
  - C r half word
  - E r word

- **index**
  - 4 r m r displacement

- **autoinc**
  - 8 r
The MIPS Instruction Format

<table>
<thead>
<tr>
<th></th>
<th>R-type</th>
<th>I-type</th>
<th>J-type</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Register</strong></td>
<td><strong>opcode</strong></td>
<td><strong>rs</strong></td>
<td><strong>rt</strong></td>
</tr>
<tr>
<td><strong>Immediate</strong></td>
<td><strong>opcode</strong></td>
<td><strong>rs</strong></td>
<td><strong>rt</strong></td>
</tr>
<tr>
<td><strong>Jump</strong></td>
<td><strong>opcode</strong></td>
<td></td>
<td><strong>target</strong></td>
</tr>
</tbody>
</table>

- The opcode tells the machine which format
**Example of instruction encoding:**

<table>
<thead>
<tr>
<th>Register R-type</th>
<th>6 bits</th>
<th>5 bits</th>
<th>5 bits</th>
<th>5 bits</th>
<th>5 bits</th>
<th>6 bits</th>
</tr>
</thead>
<tbody>
<tr>
<td>opcode</td>
<td>rs</td>
<td>rt</td>
<td>rd</td>
<td>shamt</td>
<td>funct</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Immediate I-type</th>
<th>6 bits</th>
<th>5 bits</th>
<th>5 bits</th>
<th>immediate</th>
</tr>
</thead>
<tbody>
<tr>
<td>opcode</td>
<td>rs</td>
<td>rt</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Jump J-type</th>
<th>6 bits</th>
<th></th>
<th></th>
<th>target</th>
</tr>
</thead>
<tbody>
<tr>
<td>opcode</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

```
opcode=0, rs=1, rt=2, rd=5, sa=0, funct=32
000000 00001 00010 00101 00000 100000
0x00222420
```

```
000000000001000100010101000000100000
0x00222420
```
Poll Q: Implications of the MIPS instruction format

<table>
<thead>
<tr>
<th></th>
<th>6 bits</th>
<th>5 bits</th>
<th>5 bits</th>
<th>5 bits</th>
<th>5 bits</th>
<th>6 bits</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Register</strong></td>
<td>R-type</td>
<td>opcode</td>
<td>rs</td>
<td>rt</td>
<td>rd</td>
<td>sa</td>
</tr>
<tr>
<td><strong>Immediate</strong></td>
<td>I-type</td>
<td>opcode</td>
<td>rs</td>
<td>rt</td>
<td></td>
<td>immediate</td>
</tr>
<tr>
<td><strong>Jump</strong></td>
<td>J-type</td>
<td>opcode</td>
<td></td>
<td></td>
<td></td>
<td>target</td>
</tr>
</tbody>
</table>

What is the maximum number of unique operations MIPS can encode?

3 64 127 128
Accessing the Operands

aka, what’s allowed to go here

- Operands are generally in one of two places:
  - Registers (32 options)
  - Memory ($2^{32}$ locations)

- Registers are:
  - Easy to specify
  - Close to the processor (fast access)

- The idea that we want to use registers whenever possible led to **load-store architectures**.
  - Normal arithmetic instructions only access registers
  - Only access memory with explicit loads and stores
Poll Q: Accessing the Operands

There are typically two locations for operands: registers (internal storage - $t0, $a0) and memory. In each column we have which (reg or mem) is better.

Which row is correct?

<table>
<thead>
<tr>
<th></th>
<th>Faster access</th>
<th>Fewer bits to specify</th>
<th>More locations</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>Mem</td>
<td>Mem</td>
<td>Reg</td>
</tr>
<tr>
<td>B</td>
<td>Mem</td>
<td>Reg</td>
<td>Mem</td>
</tr>
<tr>
<td>C</td>
<td>Reg</td>
<td>Mem</td>
<td>Reg</td>
</tr>
<tr>
<td>D</td>
<td>Reg</td>
<td>Reg</td>
<td>Mem</td>
</tr>
<tr>
<td>E</td>
<td>None of the above</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

[43x19]CSE 141 CC BY-NC-ND Pat Pannuto – Many slides adapted from Dean Tullsen 21
MIPS uses a load/store architecture to access operands

can do:

\[
\text{add } t0 = s1 + s2
\]

and

\[
lw \ t0, 32(s3)
\]

forces heavy dependence on registers, which is exactly what you want in today’s CPUs

can’t do

\[
\text{add } t0 = s1, 32(s3)
\]

— more instructions

+ fast implementation
  
  (e.g., easy pipelining)

What pushes MIPS towards a load/store design? (hint: fixed instruction length)
How Many Operands?  
*aka how many of these?*

- Most instructions have three operands (e.g., $z = x + y$).
- Well-known ISAs specify 0-3 (explicit) operands per instruction.
- Operands can be specified implicitly or explicitly.
Historically, many classes of ISAs have been explored, and trade off compactness, performance, and complexity.

<table>
<thead>
<tr>
<th>Style</th>
<th># Operands</th>
<th>Example</th>
<th>Operation</th>
</tr>
</thead>
<tbody>
<tr>
<td>Stack</td>
<td>0</td>
<td>add</td>
<td>(tos_{(N-1)} \leftarrow tos_{(N)} + tos_{(N-1)})</td>
</tr>
<tr>
<td>Accumulator</td>
<td>1</td>
<td>add A</td>
<td>(acc \leftarrow acc + mem[A])</td>
</tr>
<tr>
<td>General Purpose</td>
<td>3</td>
<td>add A B Rc</td>
<td>(mem[A] \leftarrow mem[B] + Rc)</td>
</tr>
<tr>
<td>Register</td>
<td>2</td>
<td>add A Rc</td>
<td>(mem[A] \leftarrow mem[A] + Rc)</td>
</tr>
<tr>
<td>Load/Store:</td>
<td>3</td>
<td>add Ra Rb Rc</td>
<td>(Ra \leftarrow Rb + Rc)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>load Ra Rb</td>
<td>(Ra \leftarrow mem[Rb])</td>
</tr>
<tr>
<td></td>
<td></td>
<td>store Ra A</td>
<td>(mem[A] \leftarrow Ra)</td>
</tr>
</tbody>
</table>
Comparing the Number of Instructions

**Code sequence for** $C = A + B$ **for four classes of instruction sets:**

<table>
<thead>
<tr>
<th>Stack</th>
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<th>GP Register (load-store)</th>
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<td></td>
<td></td>
<td>(register-memory)</td>
<td>(load-store)</td>
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Push A
Push B
Add
Pop C
Comparing the Number of Instructions

Code sequence for $C = A + B$ for four classes of instruction sets:

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</thead>
<tbody>
<tr>
<td>Push A</td>
<td>Load A</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Push B</td>
<td>Add B</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Add</td>
<td>Store C</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Pop C</td>
<td></td>
<td></td>
<td></td>
</tr>
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Comparing the Number of Instructions

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<th>GP Register</th>
<th>GP Register</th>
</tr>
</thead>
<tbody>
<tr>
<td>Push A</td>
<td>Load A</td>
<td>ADD C, A, B</td>
<td>(load-store)</td>
</tr>
<tr>
<td>Push B</td>
<td>Add B</td>
<td></td>
<td>(register-memory)</td>
</tr>
<tr>
<td>Add</td>
<td>Store C</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Pop C</td>
<td></td>
<td></td>
<td></td>
</tr>
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## Comparing the Number of Instructions

### Code sequence for $C = A + B$ for four classes of instruction sets:

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<th>GP Register</th>
<th>GP Register</th>
</tr>
</thead>
<tbody>
<tr>
<td>Push A</td>
<td>Load A</td>
<td>ADD C, A, B</td>
<td>Load R1,A</td>
</tr>
<tr>
<td>Push B</td>
<td>Add B</td>
<td></td>
<td>Load R2,B</td>
</tr>
<tr>
<td>Add</td>
<td>Store C</td>
<td></td>
<td>Add R3,R1,R2</td>
</tr>
<tr>
<td>Pop C</td>
<td></td>
<td></td>
<td>Store C,R3</td>
</tr>
</tbody>
</table>
Exercise: Working through alternative ISAs
[if time]

Stack Architecture
Accumulator
GPR
GPR (Load-store)

A = X*Y - B*C

Stack

Memory

Accumulator

A
X
Y
B
C
temp

R1
R2
R3

12
3
4
5


Poll Q: The destination of a MIPS add operation can be...

- Only the top of the stack
- Only the accumulator register
- Any general purpose register
- Any general purpose register or anywhere in memory
- Any general purpose register or the top of the stack
Addressing Modes
aka: how do we specify the operand we want?

- Register direct R3
- Immediate (literal) #25
- Direct (absolute) M[10000]
- Register indirect M[R3]
- Base+Displacement M[R3 + 10000]
- Base+Index M[R3 + R4]
- Scaled Index M[R3 + R4*d + 10000]
- Autoincrement M[R3++]
- Autodecrement M[R3 - -]
- Memory Indirect M[ M[R3] ]
MIPS addressing modes and syntax

**register direct**

```
add $1, $2, $3
```

**immediate**

```
add $1, $2, #35
```

**base + displacement**

```
lw $1, disp($2)
```

\[(R1 = M[R2 + disp])\]

**register indirect**

\[\Rightarrow\]\ disp = 0
\[\Rightarrow\]\ (rs) = 0
Is this sufficient?

- Measurements on the VAX show that these addressing modes (immediate, direct, register indirect, and base+displacement) represent 88% of all addressing mode usage.
- Similar measurements show that 16 bits is enough for the immediate 75 to 80% of the time.
- And that 16 bits is enough of a displacement 99% of the time.
- (And when these are not sufficient, it typically means we need one more instruction)
What does memory look like anyway?

- Viewed as a large, single-dimension array, with an address.
- A memory address is an index into the array
- "Byte addressing" means that the index (address) points to a byte of memory.
Memory accesses are (often) required to be “word-aligned” because of how buses and memory work

- Bytes are nice, but most data items use larger "words"
- For MIPS, a word is 32 bits or 4 bytes.

<table>
<thead>
<tr>
<th>Offset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>32 bits of data</td>
</tr>
<tr>
<td>4</td>
<td>32 bits of data</td>
</tr>
<tr>
<td>8</td>
<td>32 bits of data</td>
</tr>
<tr>
<td>12</td>
<td>32 bits of data</td>
</tr>
</tbody>
</table>

- Words are aligned
  i.e., what are the least 2 significant bits of a word address?
The MIPS ISA, so far

- fixed 32-bit instructions
- 3 instruction formats (R, I, J)
- 3-operand, load-store architecture
- 32 general-purpose registers
  - R0 always equals 0.
- 2 additional special-purpose integer registers, HI and LO, because multiply and divide produce more than 32 bits.
- registers are 32-bits wide (word)
- register, immediate, and base+displacement addressing modes
But what kinds of things do computers actually do?

• arithmetic
• logical
• data transfer
• conditional branch
• unconditional jump
Which kinds of instructions does (and doesn’t) the MIPS ISA support?

• arithmetic
  – add, subtract, multiply, divide
  – But not:

• logical
  – and, or, shift left, shift right
  – But not:

• data transfer
  – load word, store word
  – But not:
“Control Flow” describes how programs execute

- Jumps
- Procedure call (jump subroutine)
- Conditional Branch
  - Used to implement, for example, if-then-else logic, loops, etc.

- Control flow must specify two things
  - Condition under which the jump or branch is taken
  - If take, the location to read the next instruction from ("target")
Jumps are unconditional control flow. What do they look like in MIPS?

- need to be able to jump to an absolute address sometimes
- need to be able to do procedure calls and returns

<table>
<thead>
<tr>
<th>Jump</th>
<th>J-type</th>
<th>opcode</th>
<th>target</th>
</tr>
</thead>
<tbody>
<tr>
<td>Jump</td>
<td>j</td>
<td>10000</td>
<td>PC = 10000</td>
</tr>
<tr>
<td>Jump and Link</td>
<td>jal</td>
<td>20000</td>
<td>$31 = PC + 4 and PC = 20000</td>
</tr>
</tbody>
</table>
  - used for procedure calls
| Jump register | jr     | $31    | PC = $31 |
  - used for returns, but can be useful for lots of other things
  - Q: how to encode jr instruction?

Warning: Some ISAs call jumps “unconditional branches” – useful not to for MIPS
What if we want to condition the control flow? Branches.

```
do { ... ; a++; } while (a < 100);
```

- `beq` and `bne` are the only branches you need
  - `beq r1, r2, addr` => if `(r1 == r2)`: goto addr
- But other operations can be combined...
  - `slt $1, $2, $3` => if `($2 < $3)` $1 = 1; else $1 = 0
- `beq`, `bne`, `slt`, and `$zero`, can implement all fundamental conditions
  - Always, never, !=, =, >, <=, >=, <, >(unsigned), <= (unsigned), ...

```
if (i<j)
    w = w+1;
else
    w = 5;
```
How do you specify the destination of a branch/jump?

• Unconditional jumps may go long distances
  – Function calls, returns, ...

• Studies show that almost all conditional branches go short distances from the current program counter
  – loops, if-then-else, ...

• A relative address requires (many) fewer bits than an absolute address
  – e.g., `beq $1, $2, 100` => if ($1 == $2): `PC = (PC+4) + 100 * 4`
MIPS Branch and Jump Addressing Modes

- Branches (e.g., beq) use PC-relative addressing mode
  - uses fewer bits since address typically close
  - Aka: base+displacement mode, with the PC being the base

- Jumps use pseudo-direct addressing mode
  - Recall opcode is 6 bits...
    - How many bits are available for displacement? How far can you jump?
  - 26 bits of the address is in the instruction, the rest is taken from the PC.

```
6  | 26
4  | 28
```

jump destination address
### MIPS in one slide

#### MIPS operands

<table>
<thead>
<tr>
<th>Name</th>
<th>Example</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>32 registers</td>
<td>$s0-$s7, $t0-$t9, $zero, $a0-$a3, $v0-$v1, $gp, $sp, $fp, $ra, $at</td>
<td>Fast locations for data. In MIPS, data must be in registers to perform arithmetic. MIPS register $zero always equals 0. Register $at is reserved for the assembler to handle large constants.</td>
</tr>
<tr>
<td>2^30 memory words</td>
<td>Memory[0], Memory[4], ... Memory[4294967292]</td>
<td>Accessed only by data transfer instructions. MIPS uses byte addresses, so sequential words differ by 4. Memory holds data structures, such as arrays, and spilled registers, such as those saved on procedure calls.</td>
</tr>
</tbody>
</table>

#### MIPS assembly language

<table>
<thead>
<tr>
<th>Category</th>
<th>Instruction</th>
<th>Example</th>
<th>Meaning</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>Arithmetic</td>
<td>add</td>
<td>add $s1, $s2, $s3</td>
<td>$s1 = $s2 + $s3</td>
<td>Three operands; data in registers</td>
</tr>
<tr>
<td></td>
<td>subtract</td>
<td>sub $s1, $s2, $s3</td>
<td>$s1 = $s2 - $s3</td>
<td>Three operands; data in registers</td>
</tr>
<tr>
<td></td>
<td>add immediate</td>
<td>addi $s1, $s2, 100</td>
<td>$s1 = $s2 + 100</td>
<td>Used to add constants</td>
</tr>
<tr>
<td>Data transfer</td>
<td>load word</td>
<td>lw $s1, 100($s2)</td>
<td>$s1 = Memory[$s2 + 100]</td>
<td>Word from memory to register</td>
</tr>
<tr>
<td></td>
<td>store word</td>
<td>sw $s1, 100($s2)</td>
<td>Memory[$s2 + 100] = $s1</td>
<td>Word from register to memory</td>
</tr>
<tr>
<td></td>
<td>load byte</td>
<td>lb $s1, 100($s2)</td>
<td>$s1 = Memory[$s2 + 100]</td>
<td>Byte from memory to register</td>
</tr>
<tr>
<td></td>
<td>store byte</td>
<td>sb $s1, 100($s2)</td>
<td>Memory[$s2 + 100] = $s1</td>
<td>Byte from register to memory</td>
</tr>
<tr>
<td></td>
<td>load upper immediate</td>
<td>lui $s1, 100</td>
<td>$s1 = 100 * 2^16</td>
<td>Loads constant in upper 16 bits</td>
</tr>
<tr>
<td>Conditional branch</td>
<td>branch on equal</td>
<td>beq $s1, $s2, 25</td>
<td>if ($s1 == $s2) go to PC + 4 + 100</td>
<td>Equal test; PC-relative branch</td>
</tr>
<tr>
<td></td>
<td>branch on not equal</td>
<td>bne $s1, $s2, 25</td>
<td>if ($s1 != $s2) go to PC + 4 + 100</td>
<td>Not equal test; PC-relative</td>
</tr>
<tr>
<td></td>
<td>set on less than</td>
<td>slt $s1, $s2, $s3</td>
<td>if ($s2 &lt; $s3) $s1 = 1; else $s1 = 0</td>
<td>Compare less than; for beq, bne</td>
</tr>
<tr>
<td></td>
<td>set less than immediate</td>
<td>slti $s1, $s2, 100</td>
<td>if ($s2 &lt; 100) $s1 = 1; else $s1 = 0</td>
<td>Compare less than constant</td>
</tr>
<tr>
<td>Unconditional jump</td>
<td>jump</td>
<td>j 2500</td>
<td>go to 10000</td>
<td>Jump to target address</td>
</tr>
<tr>
<td></td>
<td>jump register</td>
<td>jr $ra</td>
<td>go to $ra</td>
<td>For switch, procedure return</td>
</tr>
<tr>
<td></td>
<td>jump and link</td>
<td>jal 2500</td>
<td>$ra = PC + 4; go to 10000</td>
<td>For procedure call</td>
</tr>
</tbody>
</table>
Review — Instruction Execution in a CPU

Registers

<table>
<thead>
<tr>
<th>Register</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>R0</td>
<td>0</td>
</tr>
<tr>
<td>R1</td>
<td>36</td>
</tr>
<tr>
<td>R2</td>
<td>60000</td>
</tr>
<tr>
<td>R3</td>
<td>45</td>
</tr>
<tr>
<td>R4</td>
<td>198</td>
</tr>
<tr>
<td>R5</td>
<td>12</td>
</tr>
<tr>
<td>...</td>
<td>...</td>
</tr>
</tbody>
</table>

Program Counter

20000

Instruction Buffer

Address

Memory

20000  10001100010000110100111000100000
20004  00000000011000100100000100000
80000  00000000000000000000000000111001

ALU

Load/Store Unit

out

post.addr

data
Poll Q: Work an Example

• Can we figure out the code?

```c
void
swap(int v[], int k)
{
    int temp;
    temp = v[k];
    v[k] = v[k+1];
    v[k+1] = temp;
}
```

<table>
<thead>
<tr>
<th>Operator</th>
<th>Value 1</th>
<th>Value 2</th>
<th>Value 3</th>
</tr>
</thead>
<tbody>
<tr>
<td>multi</td>
<td>$2</td>
<td>$5</td>
<td>4</td>
</tr>
<tr>
<td>add</td>
<td>$2</td>
<td>$4</td>
<td>$2</td>
</tr>
<tr>
<td>lw</td>
<td>$15, 0($2)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>lw</td>
<td>$16, 4($2)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>sw</td>
<td>$16, 0($2)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>sw</td>
<td>$15, 4($2)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>jr</td>
<td>$31</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Where is k?</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>$4</td>
</tr>
<tr>
<td>B</td>
<td>$5</td>
</tr>
<tr>
<td>C</td>
<td>$15</td>
</tr>
<tr>
<td>D</td>
<td>$16</td>
</tr>
<tr>
<td>E</td>
<td>None of the above</td>
</tr>
</tbody>
</table>
MIPS ISA Tradeoffs

What if?

- 64 registers
- 20-bit immediates
- 4 operand instruction (e.g. $Y = AX + B$)
RISC Architectures

- MIPS, like SPARC, PowerPC, and Alpha AXP, is a RISC (Reduced Instruction Set Computer) ISA.
  - fixed instruction length
  - few instruction formats
  - load/store architecture

- RISC architectures worked because they enabled pipelining. They continue to thrive because they enable parallelism.
Alternative Architectures

• Design alternative:
  – provide more powerful operations
  – goal is to reduce number of instructions executed
  – danger is a slower cycle time and/or a higher CPI (cycles per instruction)

• Sometimes referred to as “RISC vs. CISC”
  – CISC = Complex Instruction Set Computer (as alt to RISC)
  – virtually all new instruction sets since 1982 have been RISC
  – VAX: minimize code size, make assembly language easy
    instructions from 1 to 54 bytes long!

• We’ll look (briefly!) at PowerPC and 80x86

• What is ARM?
**PowerPC**

• **Indexed addressing**
  – example: \[\texttt{lw } \$t1,\$a0+\$s3 \] # \(\$t1=\text{Memory}[\$a0+\$s3]\)
  – What do we have to do in MIPS?

• **Update addressing**
  – update a register as part of load (for marching through arrays)
  – example: \[\texttt{lwu } \$t0,4(\$s3) \] # \(\$t0=\text{Memory}[\$s3+4];\$s3=\$s3+4\)
  – What do we have to do in MIPS?

• **Others:**
  – load multiple/store multiple
  – a special counter register “**bc Loop**”
  \[\texttt{bc } \textit{Loop} \]
  \(\text{decrement counter, if not 0 goto loop}\)
80x86

1978: The Intel 8086 is announced (16 bit architecture)
1980: The 8087 floating point coprocessor is added
1982: The 80286 increases address space to 24 bits, +instructions
1985: The 80386 extends to 32 bits, new addressing modes
1989-1995: The 80486, Pentium, Pentium Pro add a few instructions
           (mostly designed for higher performance)
1997: MMX is added
1999: Pentium III (same architecture)
2001: Pentium 4 (144 new multimedia instructions), simultaneous multithreading (hyperthreading)
2005: dual core Pentium processors
2006: quad core (sort of) Pentium processors
2009: Nehalem – eight-core multithreaded processors
2015: Skylake – 4-core, multithreaded, added hw security features, transactional memory...
80x86

• **Complexity:**
  – Instructions from 1 to 17 bytes long
  – one operand must act as both a source and destination
  – one operand can come from memory
  – complex addressing modes
    e.g., “base or scaled index with 8 or 32 bit displacement”

• **Saving grace:**
  – the most frequently used instructions are not too difficult to build
  – compilers avoid the portions of the architecture that are slow
Key Points

• MIPS is a general-purpose register, load-store, fixed-instruction-length architecture.
• MIPS is optimized for fast pipelined performance, not for low instruction count.
• Historic architectures favored code size over parallelism.
• MIPS most complex addressing mode, for both branches and loads/stores is base + displacement.