# WES237B - SU22 

Lab3

## Jetson TX2 - Processing Components

- Dual-core NVIDIA Denver2 + quad-core ARM Cortex-A57
- 256-core Pascal GPU
- 8GB LPDDR4, 128-bit interface
- 32GB eMMC
- 4 kp60 H.264/H. 265 encoder and decoder
- Dual ISPs (Image Signal Processors)
- 1.4 Gpps MIPI CSI camera ingest


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- Let's check the CPUs:



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- Let's check the CPUs
- Query current CPU configuration:
sudo nvpmodel -q
- Check available CPU configurations: cat /etc/nvpmodel.conf
- Set current CPU configuration:

```
sudo nvpmodel -m <id>
```



## SISD, SIMD, MIMD, \& MISD

- SISD: Single Instruction, Single Data
one processor that handles one algorithm using one source of data at a time

SISD
Instruction Pool


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multiple processors, each capable of accepting its own instruction stream independently from the others. Each processor also pulls data from a separate data stream



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- MISD: Multiple Instructions, Single Data
multiple processors. Each processor uses a different algorithm but uses the same shared input data



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MIMD $\quad$ Instruction Pool

|  | $\xrightarrow{\rightarrow \mathrm{PU}} \rightarrow \rightarrow \mathrm{PU}$ |
| :---: | :---: |
|  |  |
|  |  |
|  |  |

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## SISD on ARM

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- Example: your previous assignment ran sequentially on CPU cores

SISD Instruction Pool


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## ARM Neon Programming

- ARMv8 Neon Unit:
- Fully integrated into the processor and uses processor's resources for loop control, caching, and integer operations
- Uses 128-bit registers for SIMD processing
- It's register file is a collection of registers that can be accessed as (8, 16, 32, 64, 128)-bit registers
- Registers contain vector of elements. The same element position in the input and output registers is referred to as a lane
- Each Neon instruction results in " $n$ " parallel operation, where " $n$ " is the number of lanes


## Neon Register and Element Size



## Neon Register and Element Size



## Neon Intrinsics

- Are functions calls that compiler replaces with an (or a sequence of) appropriate Neon instruction(s)
- Functions: https://developer.arm.com/architectures/instruction-sets/simd-isas/neon/intrinsics?page=1


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- Data types:



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- Data types:
<int, uint, float, poly><64, 32, 16, $8>x<16,8,4,2,1>$ _t


| D |  |  |  |  |  | D |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| S |  | S |  |  |  | S |  |  |  | S |  |  |  |
| H | H | H |  | H |  | H |  | H |  | H |  | H |  |
| B B | B | B | B | B | B | B | B | B | B | B | B | B | B |
| Unused |  |  |  |  |  | D |  |  |  |  |  |  |  |
| Unused |  |  |  |  |  | S |  |  |  | S |  |  |  |
| Unused |  |  |  |  |  | H |  | H |  | H |  | H |  |
| Unused |  |  |  |  |  | B | B | B | B | B | B | B | B |

2D (Double word)
4S (Single word)
8H (Halfword)
16B (Byte)
1D (Double word)
4S (Single word)
4H (Halfword)
8B (Byte)

## Compile Neon

- ARMv7 (PYNQ) requires -mfpu=neon and -O1 -ftree-vectorize
- ARMv8 (Jetson) requires -01 -ftree-vectorize
- Lab Work:
- Complete neon.c (provided)
- Compile it with: gcc -mfpu=neon neon.c -o neon
- Run: ./neon


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- Lab Work:
- Complete neon.c (provided)
- Compile it with: gcc -mfpu=neon neon.c -o neon
- Run: ./neon
- Modify the code to add 250 to data instead of 3


## FIR Filtering

## 1D Convolution



## 1D Convolution

| 0000000 | Input | 0000000 |
| :--- | :--- | :--- |

Coefs

## 1D Convolution



## 1D Convolution



## 1D Convolution

- 2 nested loops
- Loop through (size of input - size of filter)
- For each filter coefficient
- Multiply by the input and accumulate
- Store result in the output



## 1D Convolution

- Complete the naive implementation in src/fir.cpp
Os Input


## Loop Unrolling

Unroll coefficient loop (inner loop) by 4 :

- Manually duplicate the single line of code
- Increment loop variable by 4


## Gprof Profiling

- Profiling tool (like perf), but will provide information on independent function calls within the executable
- Perf will only provide a cycle count and execution time for the entire executable.
- Compile flag `-pg`
- Running the executable
- There should now be a report `gmon.out` in the directory
- Make sure you remove the gmon.out if you run the program again.


## Gprof Profiling

- View the report with `gprof -b <EXEC-NAME> gmon.out - For this lab, the command is 'gprof -b lab3_fir gmon.out`
- `fir() ${ }^{\prime}$ takes up 50\% of execution time
- `fir_opt()` takes up 42.9\% of execution time

| sel | der |
| :---: | :---: |
|  |  |
| 50.0 0.288 | ${ }_{1}^{3 / 2} / 2$ |
| 42,90.0.24 | ${ }_{1}^{1 / 2}$ |
|  | 3/3 ${ }^{3 / 3}$ |
|  |  |
|  |  |
|  |  |
|  |  |
| 161) 0.0 |  |

## SIMD Instructions

- Include <arm_neon.h> (already done for the lab)
- Add compiler flag: -mfpu=neon (only on PYNQ, not on Jetson. Already done for lab)

Replace the unrolled loop body by NEON Instructions

1. Declare SIMD registers: Use 128-bits SIMD vectors
a. Float 32 -bit x 4
2. Initialize output SIMD vector with 0
3. Inside the loop:
a. Load input data into SIMD vector
b. Load coefficients into SIMD vector
c. Multiply-accumulate into output SIMD vector
4. Add 4 values together then store in output array

## Compile Comparison

- Compile the lab with the -OO compilation flag
- Run the executable and investigate the gprof report gprof -b lab3_fir gmon.out

| Call |  |  |
| :---: | :---: | :---: |
| - tue sout |  | mome |
| $\begin{array}{lll}100.0 & 0.02 & 0.76 \\ & 0.29 & 0.00 \\ & 0.24 & 0.00 \\ & 0.23 & 0.00 \\ & 0.00 & 0.00 \\ & 0.00 & 0.00\end{array}$ | $\begin{aligned} & 1 / 2 \\ & \substack{1 / 2 \\ 1 / 2 \\ 1 / 2} \end{aligned}$ |  <br>  |
|  | ${ }^{\frac{2}{2}}$ |  |
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| \% | 疗/2 |  |
|  | ${ }^{3 / 3}$ | Stamatithet 121 |
| (13) 0.00 | (2/2 | counite cin int |
|  |  |  |
|  | , |  |
|  | ${ }^{1 / 2}$ |  |
| 131) 0.0 .808 | ${ }^{\text {in }}$ |  |

## Compile Comparison

- Change the compile flag from -O0 to -01
- Run the executable and investigate the gprof report gprof -b lab3_fir gmon.out

https://linux.die.net/man/1/gcc

