CSE 141L: Introduction to Computer Architecture Lab Implementing

Pat Pannuto, UC San Diego

ppannuto@ucsd.edu

CSE 141L

CC BY-NC-ND Pat Pannuto – Content derived from materials from John Eldon, Dean Tullsen, Steven Swanson, and other

Milestone 1 is due in 7 days

- What to submit?
 - <u>SOMETHING</u>
- M1 is graded for completion, not accuracy
 - The purpose of milestones is to *help you* manage large, long-term project
 - TAs will use gradescope "grades" to help give feedback
 - Recall: Only Milestone 4 (final submission) is actual grade*
 - *With exceptions for things such as skipping milestones altogether

Today's Objectives: What does implementing look like?

- Some tips for setting up CloudLabs
- Exploring the **basic_proc** example
- Exploring ModelSim/Questa and Quartus

n.b. the rest of these slides not presented, but here as a reference

The code editors in ModelSim/Questa/Quartus aren't great

- You can use them, but more modern editors have some helpful tools
- Especially around version control
 - Because you are using version control, right?
 - And I don't mean copying folders milestone1, m1_working, m1_real, m1_final, ...

CloudLabs — What's ephemeral and what's not

- Spins up a 'fresh machine' each login
- But you have a shared L: / drive that persists across sessions
 - So put stuff there
 - But also maybe don't trust it 100%
 - [What fixes this? Version control of course!]
- Take advantage of "portable apps"
 - <u>https://code.visualstudio.com/docs/editor/portable</u>
 - <u>https://git-scm.com/download/win</u> Choose "portable" and install in L:/

Portable VSCode

- Download the **zip**, not the installer
- Unzip the folder in your L: / drive, and make a folder called data

→ * ↑	is PC ⇒	ppannuto (\\amznfsx7umcv4bw.AD.	> VSCode-win32-x64-1.63.2 >		~ Ç	Search VSCode-win32-x64-1.6 🔎	
T1: 00		Name	Date modified	Туре	Size		
This PC		bin	1/18/2022 5:29 PM	File folder			
Downloads		data	1/18/2022 5:30 PM	File folder			
Temporary Files		locales	1/18/2022 5:29 PM	File folder			
😦 ppannuto (\\amznf		resources	1/18/2022 5:29 PM	File folder			
		swiftshader	1/18/2022 5:29 PM	File folder			
		tools	1/18/2022 5:29 PM	File folder			
	[chrome_100_percent.pak	1/18/2022 5:28 PM	PAK File	139 KB		
	[chrome_200_percent.pak	1/18/2022 5:28 PM	PAK File	203 KB		
		🔇 Code	1/18/2022 5:28 PM	Application	124,394 KB		
	[Code.VisualElementsManifest	1/18/2022 5:28 PM	XML Document	1 KB		
	6	d3dcompiler_47.dll	1/18/2022 5:28 PM	Application extens	4,428 KB		
	6	🗟 ffmpeg.dll	1/18/2022 5:28 PM	Application extens	2,160 KB		
	[icudtl.dat	1/18/2022 5:28 PM	DAT File	10,170 KB		
	1	ibEGL.dll	1/18/2022 5:28 PM	Application extens	435 KB		
	1	libGLESv2.dll	1/18/2022 5:28 PM	Application extens	7,759 KB		
	[resources.pak	1/18/2022 5:29 PM	PAK File	4,766 KB		
	[snapshot_blob.bin	1/18/2022 5:29 PM	BIN File	48 KB		
	[v8_context_snapshot.bin	1/18/2022 5:29 PM	BIN File	162 KB		
	1	vk_swiftshader.dll	1/18/2022 5:29 PM	Application extens	4,585 KB		
	1	vk_swiftshader_icd	1/18/2022 5:29 PM	JSON File	1 KB		
	F	vulkan-1.dll	1/18/2022 5:29 PM	Application extens	713 KB		

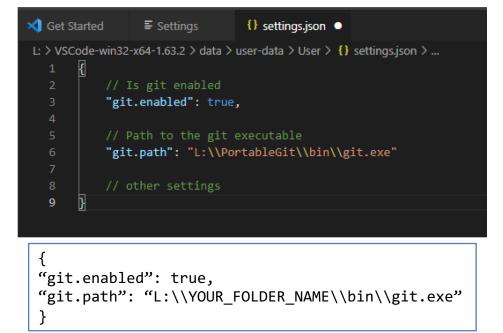


C BY-NC-ND Pat Pannuto – Content derived from materials from John Eldon, Dean Tullsen, Steven Swanson, and others

If using portable apps, have to point VSCode to git

• File->Preferences->Settings; search `git-path`; write this json:

Terminal Help		Settings - Visual Studio Code	– 🗆 X
刘 Get Started	■ Settings	x	₾ Ш …
git-path			1 Setting Found 🗮
User			Turn on Settings Sync
✓ Extensions (Git (1)	¹⁾ Ø	Git: Path (Syn:: Ignored) Path and filename of the git executable, e.g. C: \Program Files\Git\bin\git.exe (Windows). This can also be a values containing multiple paths to look up. Edit in settingsjson	



Quick reminder: No public repos please

- Q: What's really clear and indisputable evidence of sharing code?
- A: A publicly accessible repository

1411 AdulisL/CSE-141L https://github.com/AdulisL/CSE-141L.git egalipchak/cse-1411 project_1 fijs/lab2_141L Lab2 for 141L. Gin594/CSE-141L https://github.com/Gin594/CSE-141L.git () iteriani/1411 https://github.com/iteriani/1411.git jnwng/141L 141L Winter 2013 quarter code work. kunkun9811/CSE 141L https://github.com/kunkun9811/CSE 141L.git (p) michellefaustina/cse-1411 Spring 2015, Eldon. I tried to keep the finished work as unmodified as possi... rog9huang/CSE_141L https://github.com/rog9huang/CSE_141L.git 💭 Run4curry/141L idek

8

The "github" built-in won't find private repos, so you have to type the URL by hand

>git	
Git: Clone	recently used 🕄
https://github.com/ppannuto/WI22-cse141l	
Clone from URL https://github.com/ppannuto/WI22-cse1411	
Clone from GitHub	

• You can use the default 'credential helper' ("manager-core"); authorize it to github; and then it will clone

Now you're set up to code!

∢	File Edit Selection	View Go Run Te	erminal Help InstROM.sv - WI22-cse141I - Visual Studio Code
Ð	EXPLORER		≡ InstROM.sv ×
	∨ WI22-CSE141L	ចុចុខ្	basic_proc > ≡ InstROM.sv
Ω	✓ basic_proc		1 // Create Date: 15:50:22 10/02/2019
/			2 // Design Name:
90	≣ Ctrl.sv		3 // Module Name: InstROM
દુહ	≣ DataMem.sv		4 // Project Name: CSE141L
	E Definitions.sv		5 // Tool versions:
a⊳ a			6 // Description: Verilog module instruction ROM template
~	■ InstFetch.sv		7 // preprogrammed with instruction values (see case statement)
	InstROM.sv		8 //
ß	≣ LUT.sv		9 // Revision: 2020.08.08
	■ ProgCtr.sv		10 //
	≣ RegFile.sv		11 module InstROM #(parameter A=10, W=9) (
			12 input [A-1:0] InstAddress,
	■ TopLevel_tb.sv		<pre>13 output logic[W-1:0] InstOut);</pre>

Careful, you (can) have two editors open

		12 12 12 1	
L:/rep	os/WI22-cse141l/basic_proc/TopLevel_tb.sv - Default		+ 2 ×
Ln#			
1	□ // Create Date: 2017.01.25		^
2	// Design Name: TopLevel Test Bench		
3	// Module Name: TopLevel_tb.v		
4	// CSE141L		
5	<pre>// This is NOT synthesizable; use for logic</pre>		
6	<pre>L // Verilog Test Fixture created for module:</pre>	: TopLevel	
7			
8	<pre>module TopLevel_tb; // Lab 17</pre>		
9			
10	// To DUT Inputs		
11	<pre>bit Init = 'bl,</pre>		
12	Req,		
13	Clk;		
14		Warning!	
15	// From DUT Outputs	Warning! X	
16	wire Ack; // done flag		
17 18	// Instantiate the Device Under Test (DUT)	File modified outside of source editor.	
19	TopLevel DUT (
20	.Reset (Init) ,	FILE: L:/repos/WI22-cse141/basic_proc/TopLevel_tb.sv	
20	.Start (Reg) ,	You may choose to:	
22	.Clk (Clk)	1) OVERWRITE disk changes with current editor content	
23	.Ack (Ack)	2) RELOAD the changes from disk	
24	-);	3) IGNORE the difference	
25			
26	initial begin	Overwrite Reload Ignore	
27	#10ns Init = 'b0;		
28	#10ns Reg = 'b1;		
29			
30	// launch prodvgram in DUT		
- 91	410mg Bog = 0.		~
<			<u> </u>
ALU.s	sv 🗙 🗋 ALU_tb.sv 🗙 📄 Ctrl.sv 🗶 📄 DataMem.sv 🗶 📄	Definitions.sv 🗴 🚺 InstFetch.sv 🗶 🔄 InstROM.sv 🗶 📄 LUT.sv 🗶 📄 ProgCtr.sv 👘 RegFile.sv 🗶 🚺 TopLevel.sv 🗶 🚺 TopLevel.sv	tb.sv ×

[Demo Plan]

- Create new project from basic_proc
- Compile
 - Show warnings; explore ALU 1 vs 1'b1
- Go to waveform viewer
 - Show results
 - Work examples / take Q's