CSE 141L: Introduction to Computer Architecture Lab
Alternative Tools

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Milestone 3 is due in 2 weeks

- What to submit?
  - SOMETHING

- M3 is something of a ‘catchup’ milestone
  - Released an example assembler on canvas; hopefully fast to adapt

- This also means you have a moment to breathe, make changes if needed

Today's Objectives:

- Introduce alternative (and open source!) tools
  - Pros: Free, easy to install
  - Cons: Slightly less user friendly ("parse error."), no GUIs, some SV not impl'd
  - Limitations: Simulation only

- Icarus Verilog

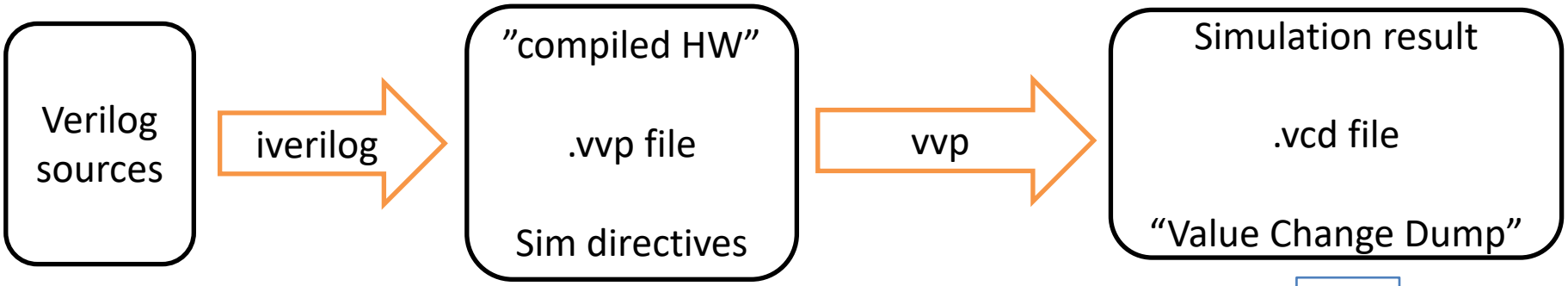
- GTKWave

Wait, do I have to install and learn even more tools?

- No.
- But they may be helpful
- At this point, you have everything you need to finish the project
  - Remaining lectures/demos are tools, tips, and Q&A time

Simulation Flow

- Questa/ModelSim follow same steps
  - They use **`vcs + vsim`**, the Cadence toolchain; can see commands in logs




```
T_3.1 ;
    %delay 1000, 0;
    %pushi/vec4 0, 0, 1;
    %store/vec4 v0x6000022c46c0_0, 0, 1;
    %vpi_call/w 3 62 "$display", "Checking that nothing happens before Start" {0 0 0};
    %load/vec4 v0x6000022c47e0_0;
```

```
#1000
0-
b0 ,
b0 !
b0 +
b1 &
1%
```

Next, you view the result of simulation

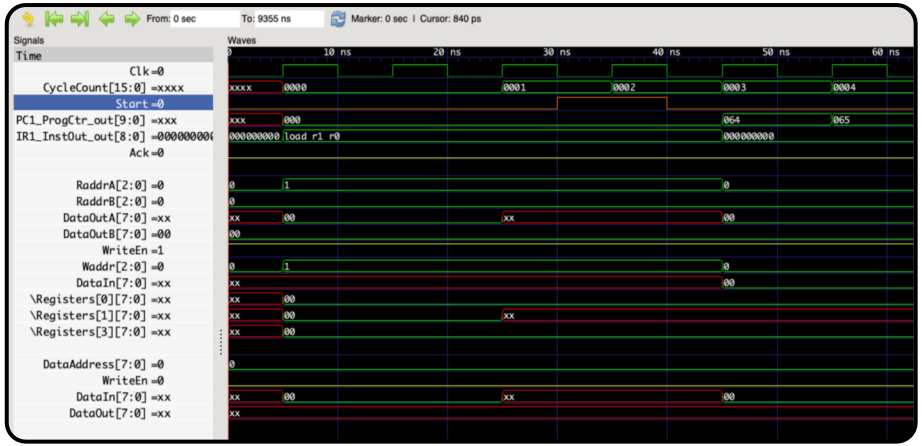
- Simulation and viewing results (waveforms) are totally decoupled
  - This is why you're hitting 'reset' all the time in ModelSim

Simulation result

.vcd file

"Value Change Dump"

GTKWave



Icarus Verilog

- Very impressive piece of OSS
  - Made and maintained by a small core for decades
- Stricter than VCS toolchain
  - Does what the spec says and only what the spec says (except in rare cases)
  - Good and bad: sometimes catches bugs, sometimes kind of annoying
- Simulation only
  - Might find documentation claiming it does synthesis; not since ~v0.8 / 2006

GTKWave

- Another impressive piece of OSS with 20+ year history
- Displays VCD (and many other) files as waveforms
- Has some nice ergonomics

The ModelSim/Questa GUI generates dump configuration based on the waveform sensitivity list

- With Icarus, needs to be done in testbench code:

```
initial begin
  $dumpfile("alu.vcd");
  $dumpvars(); // Just dump everything
  $dumplimit(104857600); // 2**20*100 = 100 MB, plenty.
end
```

Icarus usage
[demo]

```
$ iverilog -Winfloop -o basic_proc.vvp -tvvp -g2012
Definitions.sv ALU.sv Ctrl.sv DataMem.sv InstROM.sv
LUT.sv ProgCtr.sv RegFile.sv TopLevel.sv TopLevel_tb.sv
Ctrl.sv:42: sorry: constant selects in always_* processes
are not currently supported (all bits will be included).
ALU.sv:25: sorry: constant selects in always_* processes
are not currently supported (all bits will be included).
ALU.sv:25: sorry: constant selects in always_* processes
are not currently supported (all bits will be included).

$
```

Icarus usage [demo]

```
$ ./basic_proc.vvp
VCD info: dumpfile basic_proc.vcd opened for output.
VCD warning: $dumpvars: Unsupported argument type (vpiPackage)
VCD warning: $dumpvars: Unsupported argument type (vpiPackage)
VCD warning: array word TopLevel_tb.DUT.RF1.Registers[0] will conflict with an escaped identifier.
VCD warning: array word TopLevel_tb.DUT.RF1.Registers[1] will conflict with an escaped identifier.
VCD warning: array word TopLevel_tb.DUT.RF1.Registers[2] will conflict with an escaped identifier.
VCD warning: array word TopLevel_tb.DUT.RF1.Registers[3] will conflict with an escaped identifier.
VCD warning: array word TopLevel_tb.DUT.RF1.Registers[4] will conflict with an escaped identifier.
VCD warning: array word TopLevel_tb.DUT.RF1.Registers[5] will conflict with an escaped identifier.
VCD warning: array word TopLevel_tb.DUT.RF1.Registers[6] will conflict with an escaped identifier.
VCD warning: array word TopLevel_tb.DUT.RF1.Registers[7] will conflict with an escaped identifier.
1000_0000
----------------------------------------
0e00_0000
last instruction =    5 || sim time              9345000
```

GTKWave usage [demo]

- Did you notice this trick earlier?