# Demo: Ultra-Constrained Sensor Platform Interfacing

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## ABSTRACT

In this work we expose the challenges of interfacing both conventional and new systems with an extremely resource constrained platform. We find that even when attempts are made to utilize an industry standard protocol (I2C), necessary protocol modifications for ultra-low power design means that interfacing remains non-trivial.

We present a functional 0.4mm x 0.8mm ARM Cortex M0 with 3KB of RAM, 24 GPIOs, and an ultra-low power I2C interface. This chip is part of the Michigan Micro Mote (M3) project, which is designed to build a complete software and hardware platform for general purpose sensing at the millimeter scale. We demo an I2C interface circuit allowing commercial hardware to program and interact with the chip and present the beginning of the millimeter scale sensing revolution.

## Categories and Subject Descriptors

B.4.3 [**HARDWARE**]: Input/Output and Data Communications—*Interconnections (subsystems)*

## Keywords

Smart Dust, low power, bus protocols

## 1. INTRODUCTION

In the design of ultra-low power systems, communication is of paramount importance. While great emphasis is often placed on *inter*-node communication – via wireless, light, et al – the challenges of *intra*-node communication are often neglected. Traditionally, this issue is relegated to existing solutions such as I2C or SPI. However, there are several important limitations when working in this space. A significant concern for our design is wire count as the integrated configuration has very limited physical space for interchip bond wires. In addition, common open-drain bus architectures impose a relatively high constant leakage through their pull-up resistors, bounded in the other extreme by maintaining a reasonably fast bus frequency. Despite these challenges, we find it undesirable and unnecessary to impose a completely novel protocol on system designers. Instead we preserve the semantics of the I2C protocol, while developing a significantly more power efficient implementation.


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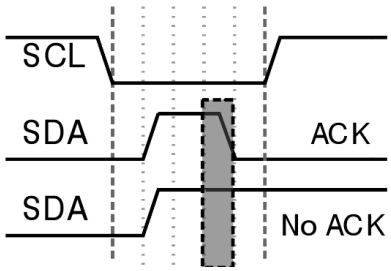



Figure 1: The ACK cycle of the modified I2C protocol. The negative clock edge is divided into 5 cycles: wait, pulse up, wait, pulse data, wait. These cycles are all 250ns long, permitting any clock rate up to 400kHz. The shaded region marks the only period in a I2C transaction the slave is responsible for driving.

### 1.1 Ultra-low Power I2C

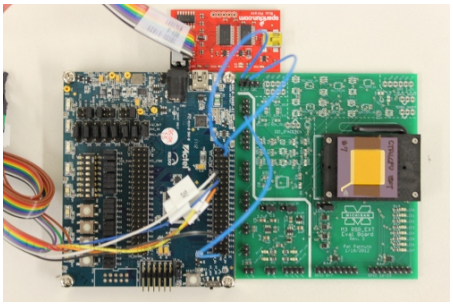
The M3 system developed an ultra-low power I2C variant. Instead of the traditional pull-up resistor, a weak keeper circuit made up of a pair of inverters preserves the current value of the clock and data lines. During communication, the I2C master is responsible for pulsing the clock line both high and low. The negative clock cycle is divided into 5 separate states: wait, pulse high, wait, pulse data, wait. The master is responsible for driving the SDA line high every cycle, allowing either the master or slave to pull down the SDA line as appropriate. A waveform of the more-interesting ACK cycle (which requires a slave device to drive the SDA line) is shown in Figure 1.

## 2. MICHIGAN MICRO MOTE

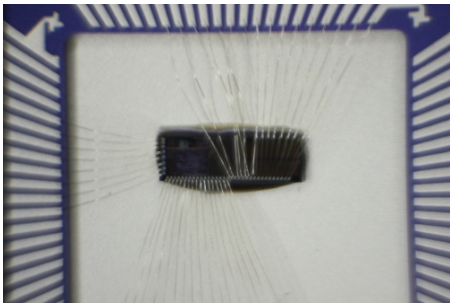
The Michigan Micro Mote (M3) project is a collaborative effort seeking to develop a general purpose millimeter-scale sensor platform [2]. The current work builds a five chip stack composed of a 96x96 pixel imager, solar energy harvester, a control CPU with 3KB of retentive memory, a DSP CPU with 16KB of non-retentive memory, energy storage, and an Ultra Wideband radio.

### 2.1 M3 as a Platform

The main utility of M3 is as a development platform for new sensors and systems. It provides the buiding blocks for the creation of a diverse array of sensors at the millimeter scale. Much like the development of the Epic core faciliatated the rapid development and deployment of sensors at the several inch scale [1], it is our hope that the M3 plat-



(a) The complete system: A commercial I2C device the BusPirate (top), the interface circuit realized in an IGLOO nano FPGA (left), and a breakout of the M3 control CPU board (right)



(b) A die shot of the M3 control CPU board

Figure 2: The ultra-low power and commerical devices

form can springboard a new class of sensors at the millimeter scale. The ultra-low power I2C to commercial I2C bridge presented in this work will allow for iterative development and utilization of the M3 platform immediately with existing hardware and enable other hardware devices to utilize our ultra-low power I2C variant.

# 3. INTERFACE

Figure 3 gives a high level overview of the differing I2C implementations. The following sections highlight the challenges of interfacing these two distinct I2C designs.

## 3.1 A Purely Combinational Approach

Our first interface attempt was the combinational circuit presented in Figure 4. The circuit latched who had pulled

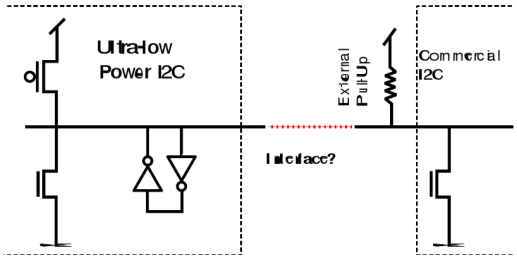



Figure 3: Two incompatible I2C implementations. Extreme care must be taken to not overpower the weak keeper. Driving signals to the low-power side requires manually driving the SDA line high both when writing and reading.

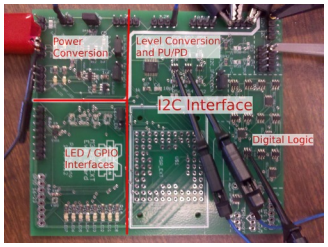



Figure 4: A combinational approach to interfacing the two divergent I2C systems. The M3 pull-up signal is supplied to a monostable multivibrator acting as a one-shot timer

a line low and held the opposite signal line low until it was released, using a one-shot timer to pulse the M3 signal lines high when the commercial chip was the master.

While nearly correct, this circuit suffered from an insurmountable timing glitch. If the commercial line was acting as the master and the LSB of a transaction was 0, it would not pulse the SDA line high until the pull-up resistor had pulled the line high, typically between 550 and 800ns after the negative edge. Referring back to Figure 1, this would cause the SDA pull-up to drown out the M3's attempt to acknowledge the transaction. In addition to the RC delay, a further 50ns of delay came from a level converter and the discrete logic components. As more challenges became apparent, it became clear that a purely combinational circuit would have been untenably complex.

## 3.2 Enter the FPGA

Our final solution takes the form of a state machine realized in an Actel IGLOO Nano FPGA. The state machine is able to act as a 'proper' M3 master, pulsing the SDA line high 250–500ns after each falling clock edge. Care must be taken while communicating from the M3 to the commercial side as well. Since the M3 data is not available until 1000ns after the negative clock edge, it leaves only 250ns to drive the commercial I2C network. In practice this requires the FPGA to hold the commercial line at about half voltage and actively drive it high or low for the last 250ns to ensure timing constraints are met.

# 4. DEMONSTRATION

In this demo, we present a functional 0.4mm x 0.8mm ARM Cortex M0 with an ultra-low power I2C network interfaced to traditional commercial I2C components. We will show bus-based DMA programming of the M3 chip using commercial I2C interfaces and communication with commercial sensors not yet adapted or optimized for millimeter scale computing, including a TI TMP101 temperature sensor.

# 5. REFERENCES

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