COMPUTER SCIENCE AND ENGINEERING
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Ultra-Constrained Sensor Platform Interfacing

Pat Pannuto <ppannuto@umich.edu>
Yoonmyung Lee, Ben Kempke, Dennis Sylvester, David Blaauw, and Prabal Dutta

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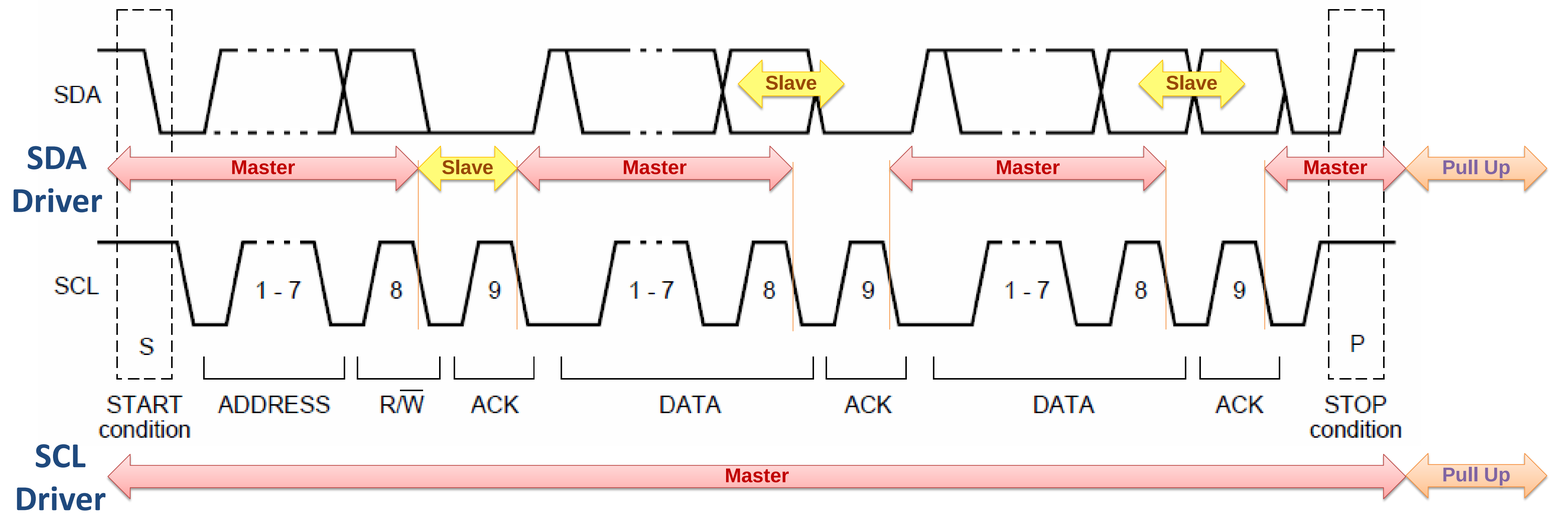
Introduction

As we continue to drive towards smaller, more constrained devices, traditional approaches to platform design and interoperability begin to break down.

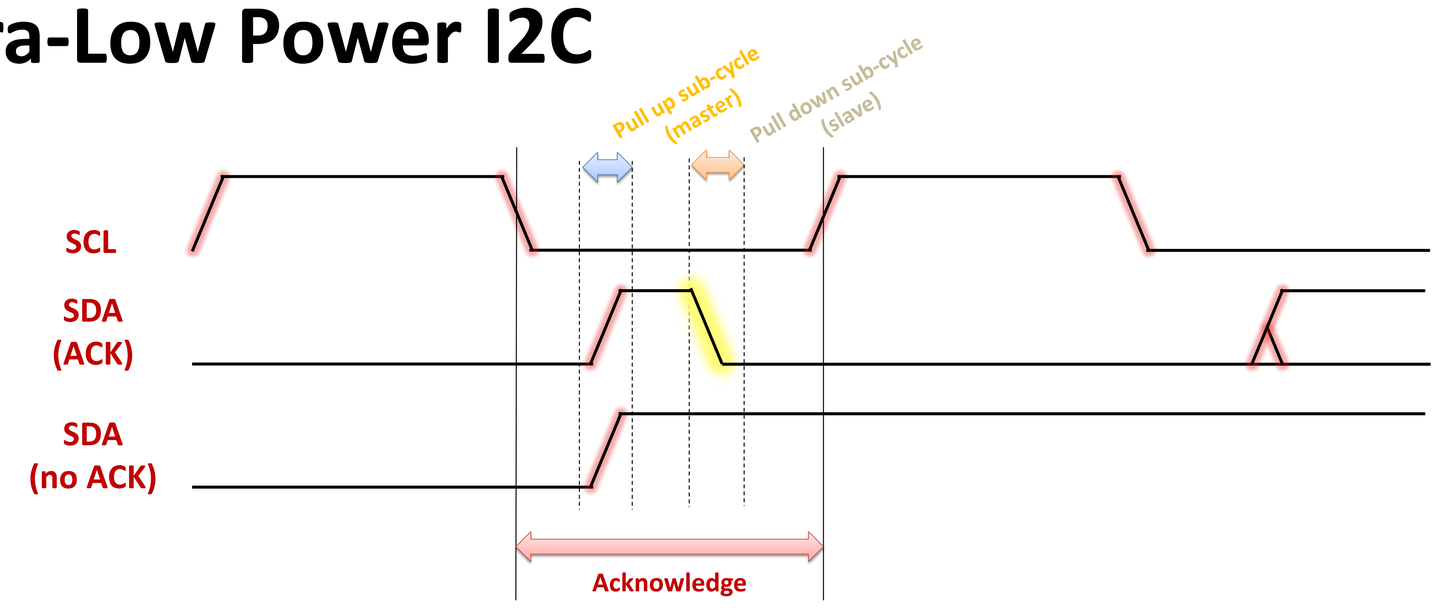
In the effort toward millimeter-scale computing, we present a fully functional Cortex M0 in a 0.4 x 0.8 mm package. We demonstrate a novel ultra-low power I2C variant and an interface circuit to communicate with it. We further discuss the challenges of interfacing traditional components with ultra-low power hardware.

This chip is part of the Michigan Micro Mote (M3) project, an effort to develop and distribute a millimeter-scale sensor platform.

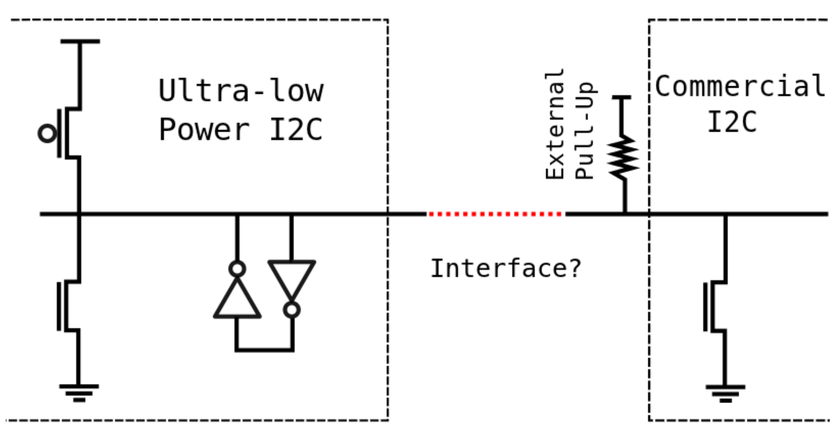
Traditional I2C

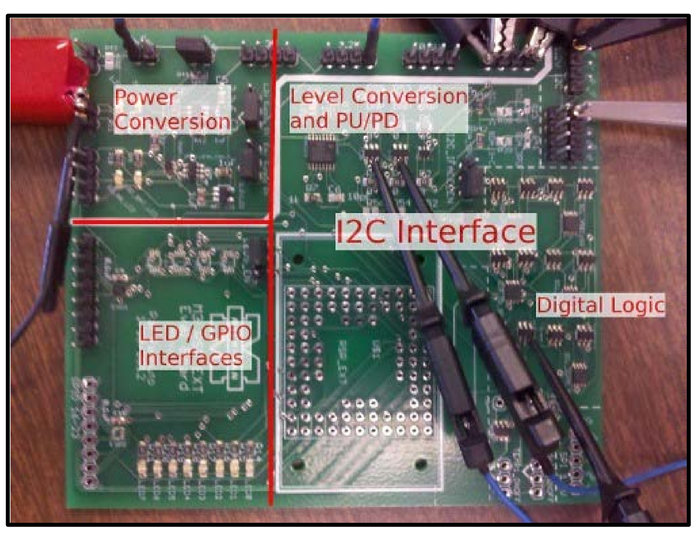


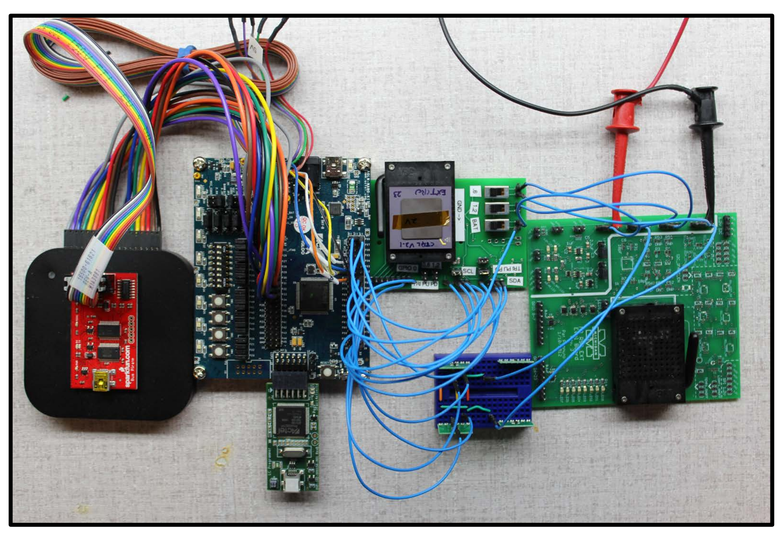
Ultra-Low Power I2C



Interfacing







Two incompatible I2C implementations

Extreme care must be taken to not overpower the weak keeper.

As a master, driving signals to the low-power side requires manually driving the SDA line high both when writing and reading.

As a slave, the interface must accommodate the late settle of the SDA line, which stabilizes only 250 ns before the next rising clock pulse at 400 kHz.

A Purely Combinational Approach

Early intuition built a simple state machine, detecting I2C START and STOP conditions to control which side's interface was sensed and which was driven. A one-shot timer replicated the SDA pull-up pulse.

Simple state machines were unable to support all the nuances of I2C, and no direct analog conversion achieved sufficiently low leakage.

Enter the FPGA

The final interface circuit uses an FPGA to implement an I2C state machine. The interface board requires two FETs as the 110 nA PFET leakage is too large for M3.